奇美電子
CHIMEI INNOLUX

PRODUCT SPECIFICATION

☐ Tentative Specification

☐ Preliminary Specification

■ Approval Specification

MODEL NO.: V546H1

SUFFIX: PS1

Customer:

APPROVED BY   SIGNATURE

Name / Title

Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
Chao-Chun Chung	Ken Wu	YI-CHEN Chiang

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REVISION HISTORY

Version	Date	Page (New)	Section	Description
C1(2.0)	Jan.21,11	all	all	Approval Specification Ver 2.0 was first issued.

Version 2.0   4   Date：24 Jan 2011

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1. GENERAL DESCRIPTION

1.1 OVERVIEW

V546H1-PS1 is a 54.6" TFT Liquid Crystal Display product with driver ICs and 4ch-LVDS interface. This product supports 1920 x 1080 HDTV format and can display true 1.073G colors (8-bit + Hi-FRC /color). The backlight unit is not built in.

1.2 FEATURES

CHARACTERISTICS ITEMS	SPECIFICATIONS
Screen Diagonal [in]	54.6
Pixels [lines]	1920 $\times$ 1080
Active Area [mm]	1209.6(H) x 680.4(V) (54.6" diagonal)
Sub-Pixel Pitch [mm]	0.21(H) x 0.63(V)
Pixel Arrangement	RGB vertical stripe
Weight [g]	3450
Physical Size [mm]	1251.4(W) x 737(H) x 1.75(D) Typ
Display Mode	Transmissive mode / Normally black
Contrast Ratio	6000:1 Typ. (Typical value measured at CMI's module)
Glass thickness (Array / CF) [mm]	0.7 / 0.7
Viewing Angle (CR>20)	+88/-88(H),+88/-88(V) Typ. (Typical value measured at CMI's module)
Color Chromaticity	R=(0.654, 0.325) G=(0.290, 0.598) B=(0.143, 0.0489) W=(0.308, 0.359) * Please refer to "color chromaticity" on 7.2
Cell Transparency [%]	5.3%Typ. (Typical value measured at CMI's module)
Polarizer Surface Treatment	Anti-Glare coating (11% Low Haze) Hardness (3H)

1.3 MECHANICAL SPECIFICATIONS

Item	Min.	Typ.	Max.	Unit	Note
Weight	-	3450	-	g	-
I/F connector mounting position	The mounting inclination of the connector makes the screen center within $\pm$ 0.5mm as the horizontal.				(2)

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Connector mounting position
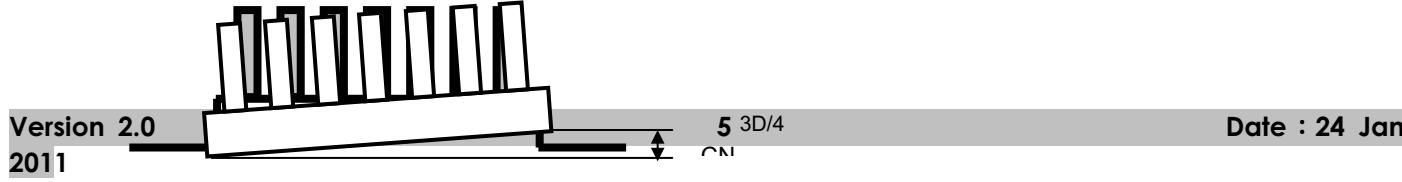
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2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	TST	-20	+60	ºC	(1) With CMI Module
Operating Ambient Temperature	TOP	0	50	ºC	(1), (2) With CMI Module

Note (1)Temperature and relative humidity range is shown in the figure below.

　　　　(a) 90 %RH Max. (Ta $\leqq$ 40 ºC).

　　　　(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

　　　　(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.

Relative Humidity (%RH)
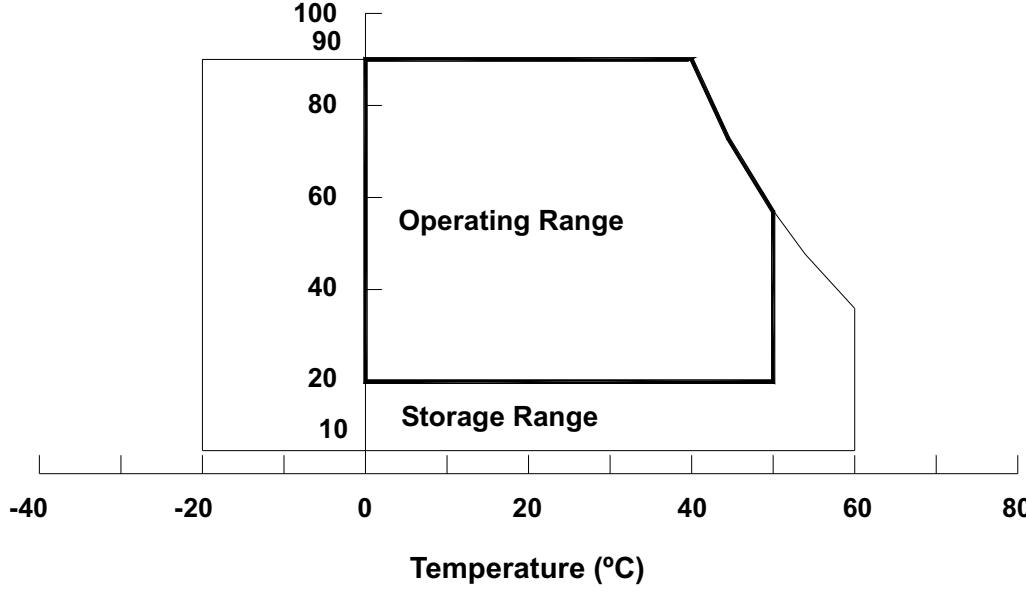
Temperature (ºC)

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2.2 ELECTRICAL ABSOLUTE RATINGS(OPEN CELL)

Storage Condition: With shipping package.

Storage temperature range: 25±5 ℃

Storage humidity range: 50±10%RH

Shelf life: a month

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD Open Cell

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Voltage for gate driver	VGH	-0.3	40	V	
Voltage for gate driver	VGL	-20	0.3	V	
Voltage range for gate driver	VGH - VGL	-0.3	43	V	
Voltage for data diver	VAA	12	18	V	
Logic Input Voltage	VIN	-0.3	5	V	

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3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD Module

(Ta = 25 ± 2 ℃)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12	13.2	V	(1)
Rush Current		I_{RUSH}	—	—	4.4	A	(2)
Power Consumption	White Pattern	—	—	7.2	8.4	W	(3)
	Horizontal Stripe	—	—	16.8	20.4	W	
	Black Pattern	—	—	6.96	8.16	W	
Power Supply Current	White Pattern	—	—	0.6	0.7	A	
	Horizontal Stripe	—	—	1.4	1.7	A	
	Black Pattern	—	—	0.58	0.68	A	
LVDS interface	Differential Input High Threshold Voltage	V_{LVTH}	+100	—	—	mV	(4)
	Differential Input Low Threshold Voltage	V_{LVTL}	—	—	-100	mV	
	Common Input Voltage	V_{CM}	1.0	1.2	1.4	V	
	Differential input voltage (single-end)	$|V_{ID}|$	200	—	600	mV	
	Terminating Resistor	R_T	—	100	—	ohm	
CMIS interface	Input High Threshold Voltage	V_{IH}	2.7	—	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	—	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition:

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+12V

Q1   Si4485DY

Vcc
(LCD Module Input)

Fuse

C3
1uF

R1
1k

VR1
47k

(Low to High)
Control Signal

SW

R2
1k

Q2
2N7002

C1
0.01uF

Vcc rising time is 470us

Vcc

0.9Vcc

0.1Vcc

GND
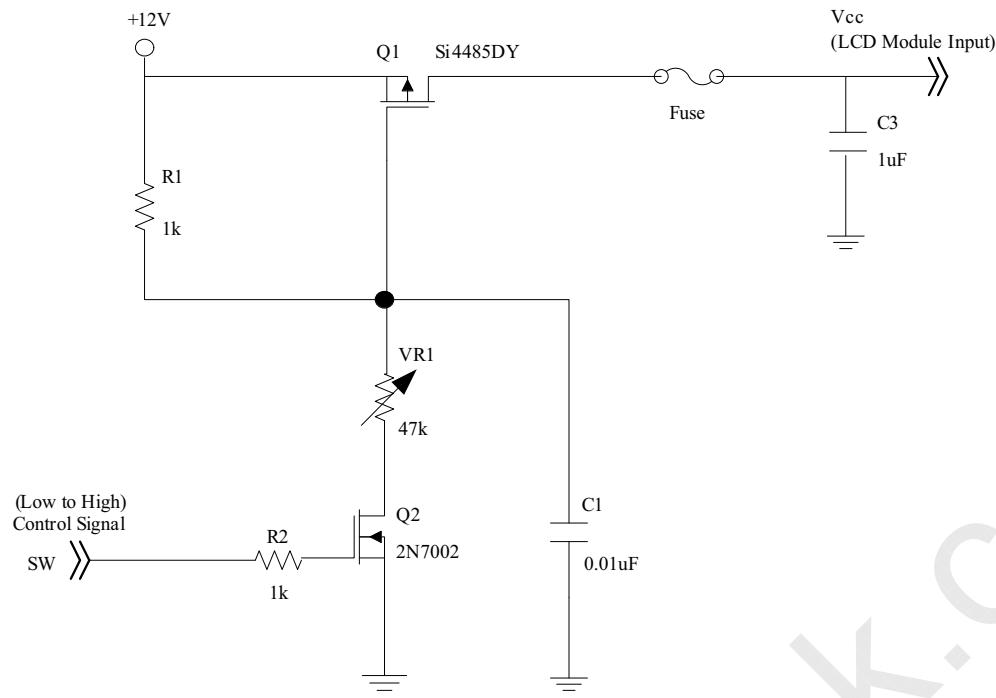
470us
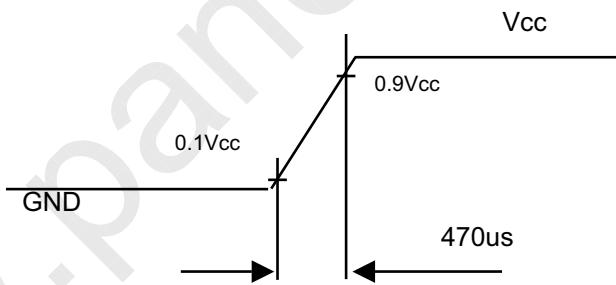
Note (3) The specified power consumption and power supply current is under the conditions at Vcc = 12 V, Ta = 25 ± 2 ºC, f_v = 120 Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern

Active Area

b. Black Pattern
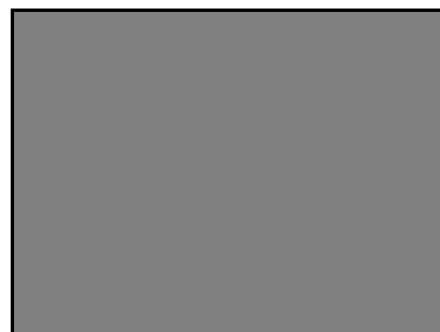
Active Area

c. Horizontal Pattern
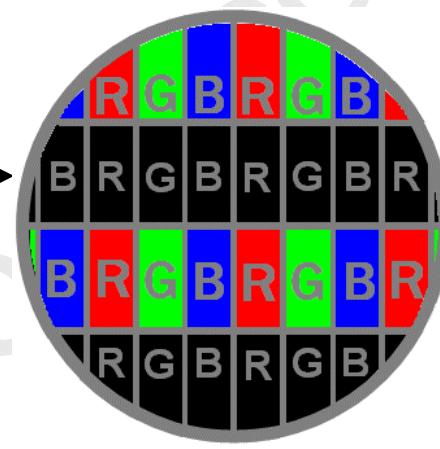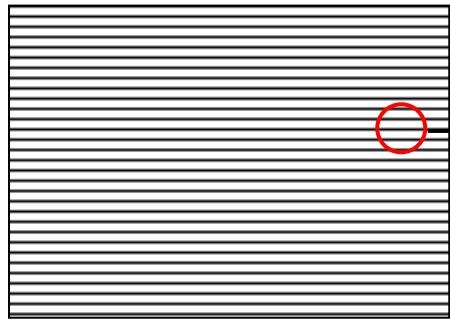
Note (4) The LVDS input characteristics are as follows:

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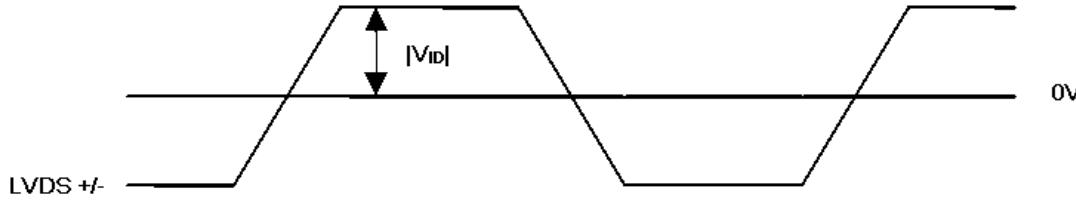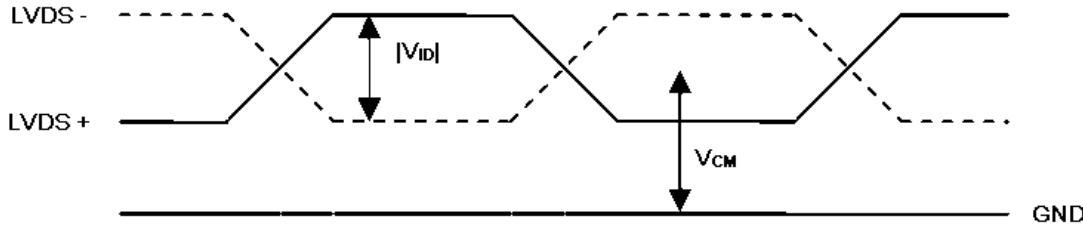
4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE

CH3_0(+/-)
CH3_1(+/-)
CH3_2(+/-)
CH3_3(+/-)
CH3_4(+/-)
CH3_CLK(+/-)

CH4_0(+/-)
CH4_1(+/-)
CH4_2(+/-)
CH4_3(+/-)
CH4_4(+/-)
CH4_CLK(+/-)

INPUT CONNECTOR CNF2: FI-RE41S-HF,JAE, or equivalent

TIMING CONTROLLER

SCAN DRIVER

TFT LCD PANEL (1920x3x1080)

CH1_0(+/-)
CH1_1(+/-)
CH1_2(+/-)
CH1_3(+/-)
CH1_4(+/-)
CH1_CLK(+/-)

CH2_0(+/-)
CH2_1(+/-)
CH2_2(+/-)
CH2_3(+/-)
CH2_4(+/-)
CH2_CLK(+/-)

SELLVDS
2D/3D
LR
LD_EN
VCC
GND
L/R_O

INPUT CONNECTOR CNF1: FI-RE51S-HF,JAE, or equivalent

DC/DC CONVERTER & REFERENCE VOLTAGE

DATA DRIVER

L/R_O

OUTPUT CONNECTOR CN6:LM123S-010-H-TF1-3 or equivalent

VBL
GND
ERR
E_PWM
BLON

CONVERTER CONNECTOR

CN1: S14B-PH-SM4-TB (JST) or CI0114M1HR0-LA (CvilLux)

CN2: CI0113M1HR0-LA (CvilLux)

CN3: CI0112M1HR0-LA (CvilLux)

LED BACKLIGHT UNIT

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5 .INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD OPEN CELL

CNF1 Connector Pin Assignment: (FI-RE51S-HF(JAE) or equivalent)

Pin	Name	Description	Note
1	N.C.	No Connection	(1)
2	N.C.	No Connection	
3	N.C.	No Connection	
4	N.C.	No Connection	
5	L/R_O	Output signal for Left Right Glasses control	(9)
6	N.C.	No Connection	(1)
7	SELLVDS	LVDS Data Format Selection	(2)(6)
8	N.C.	No Connection	(1)
9	N.C.	No Connection	
10	N.C.	No Connection	
11	GND	Ground	
12	CH1[0]-	First pixel Negative LVDS differential data input. Pair 0	(8)
13	CH1[0]+	First pixel Positive LVDS differential data input. Pair 0	
14	CH1[1]-	First pixel Negative LVDS differential data input. Pair 1	
15	CH1[1]+	First pixel Positive LVDS differential data input. Pair 1	
16	CH1[2]-	First pixel Negative LVDS differential data input. Pair 2	
17	CH1[2]+	First pixel Positive LVDS differential data input. Pair 2	
18	GND	Ground	
19	CH1CLK-	First pixel Negative LVDS differential clock input.	(8)
20	CH1CLK+	First pixel Positive LVDS differential clock input.	
21	GND	Ground	
22	CH1[3]-	First pixel Negative LVDS differential data input. Pair 3	(8)
23	CH1[3]+	First pixel Positive LVDS differential data input. Pair 3	
24	CH1[4]-	First pixel Negative LVDS differential data input. Pair 4	
25	CH1[4]+	First pixel Positive LVDS differential data input. Pair 4	
26	2D/3D	Input signal for 2D/3D Mode Selection	(3)(7)
27	L/R	Input signal for Left Right eye frame synchronous	(4)(7)

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28	CH2[0]-	Second pixel Negative LVDS differential data input. Pair 0	(8)
29	CH2[0]+	Second pixel Positive LVDS differential data input. Pair 0	(8)
30	CH2[1]-	Second pixel Negative LVDS differential data input. Pair 1	
31	CH2[1]+	Second pixel Positive LVDS differential data input. Pair 1	(8)
32	CH2[2]-	Second pixel Negative LVDS differential data input. Pair 2	
33	CH2[2]+	Second pixel Positive LVDS differential data input. Pair 2	
34	GND	Ground	
35	CH2CLK-	Second pixel Negative LVDS differential clock input.	(8)
36	CH2CLK+	Second pixel Positive LVDS differential clock input.	
37	GND	Ground	
38	CH2[3]-	Second pixel Negative LVDS differential data input. Pair 3	
39	CH2[3]+	Second pixel Positive LVDS differential data input. Pair 3	(8)
40	CH2[4]-	Second pixel Negative LVDS differential data input. Pair 4	
41	CH2[4]+	Second pixel Positive LVDS differential data input. Pair 4	
42	LD_EN	Input signal for Local Dimming Enable	(5)(7)
43	N.C.	No Connection	(1)
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	N.C.	No Connection	(1)
48	VCC	+12V power supply	
49	VCC	+12V power supply	
50	VCC	+12V power supply	
51	VCC	+12V power supply	

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CNF2 Connector Pin Assignment (FI-RE41S-HF (JAE) or equivalent)

Pin	Name	Description	Note
1	N.C.	No Connection	(1)
2	N.C.	No Connection	
3	N.C.	No Connection	
4	N.C.	No Connection	
5	N.C.	No Connection	
6	N.C.	No Connection	
7	N.C.	No Connection	
8	N.C.	No Connection	
9	GND	Ground	
10	CH3[0]-	Third pixel Negative LVDS differential data input. Pair 0	(8)
11	CH3[0]+	Third pixel Positive LVDS differential data input. Pair 0	
12	CH3[1]-	Third pixel Negative LVDS differential data input. Pair 1	
13	CH3[1]+	Third pixel Positive LVDS differential data input. Pair 1	
14	CH3[2]-	Third pixel Negative LVDS differential data input. Pair 2	
15	CH3[2]+	Third pixel Positive LVDS differential data input. Pair 2	
16	GND	Ground	
17	CH3CLK-	Third pixel Negative LVDS differential clock input.	(8)
18	CH3CLK+	Third pixel Positive LVDS differential clock input.	
19	GND	Ground	
20	CH3[3]-	Third pixel Negative LVDS differential data input. Pair 3	(8)
21	CH3[3]+	Third pixel Positive LVDS differential data input. Pair 3	
22	CH3[4]-	Third pixel Negative LVDS differential data input. Pair 4	
23	CH3[4]+	Third pixel Positive LVDS differential data input. Pair 4	
24	GND	Ground	
25	GND	Ground	
26	CH4[0]-	Fourth pixel Negative LVDS differential data input. Pair 0	(8)
27	CH4[0]+	Fourth pixel Positive LVDS differential data input. Pair 0	
28	CH4[1]-	Fourth pixel Negative LVDS differential data input. Pair 1	

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29	CH4[1]+	Fourth pixel Positive LVDS differential data input. Pair 1	
30	CH4[2]-	Fourth pixel Negative LVDS differential data input. Pair 2	
31	CH4[2]+	Fourth pixel Positive LVDS differential data input. Pair 2	(8)
32	GND	Ground	
33	CH4CLK-	Fourth pixel Negative LVDS differential clock input.	(8)
34	CH4CLK+	Fourth pixel Positive LVDS differential clock input.	
35	GND	Ground	
36	CH4[3]-	Fourth pixel Negative LVDS differential data input. Pair 3	
37	CH4[3]+	Fourth pixel Positive LVDS differential data input. Pair 3	(8)
38	CH4[4]-	Fourth pixel Negative LVDS differential data input. Pair 4	
39	CH4[4]+	Fourth pixel Positive LVDS differential data input. Pair 4	
40	GND	Ground	
41	GND	Ground	

CN6 Connector Pin Assignment (LM123S-010-H-TF1-3 (UNE) or equivalent)

1	N.C.	No Connection	
2	N.C.	No Connection	(1)
3	N.C.	No Connection	
4	GND	Ground	
5	N.C.	No Connection	(1)
6	L/R_O	Output signal for Left Right Glasses control	(9)
7	N.C.	No Connection	
8	N.C.	No Connection	(1)
9	N.C.	No Connection	
10	N.C.	No Connection	

Note (1) Reserved for internal use. Please leave it open.

Note (2) LVDS format selection.

   L= Connect to GND, H=Connect to +3.3V or open

SELLVDS	Note
L	JEIDA Format
H or Open	VESA Format

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Note (3) 2D/3D mode selection.

L= Connect to GND or Open, H=Connect to +3.3V

2D/3D	Note
L or Open	2D Mode
H	3D Mode

Note (4) Input signal for Left Right eye frame synchronous

V_{IL}=0~0.8 V, V_{IH}=2.0~3.3 V

| L/R	Note
L	Right synchronous signal
H	Left synchronous signal

Note (5) Local dimming enable selection.

L= Connect to GND or Open, H=Connect to +3.3V

LD_EN	Note
L or Open	Local Dimming Disable
H	Local Dimming Enable

Note (6) SELLVDS signal pin connected to the LCM side has the following diagram.

R1 in the system side should be less than 1K Ohm. (R1 < 1K Ohm)
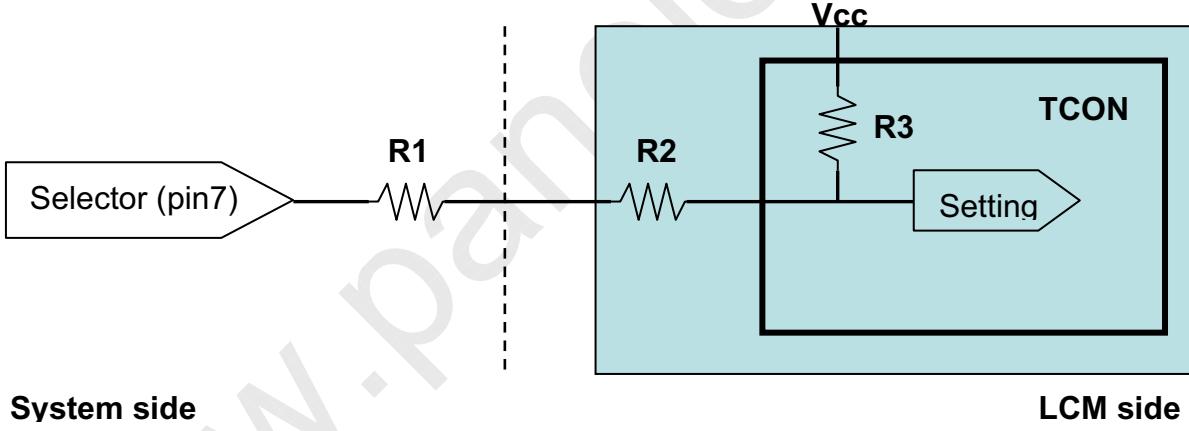
System side　　　　　　　　　　　　　**LCM side**

System side
R1 < 1K

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Note (7) 2D/3D, L/R and LD_EN signal pin connected to the LCM side has the following diagram.

R1 in the system side should be less than 1K Ohm. (R1 < 1K Ohm)
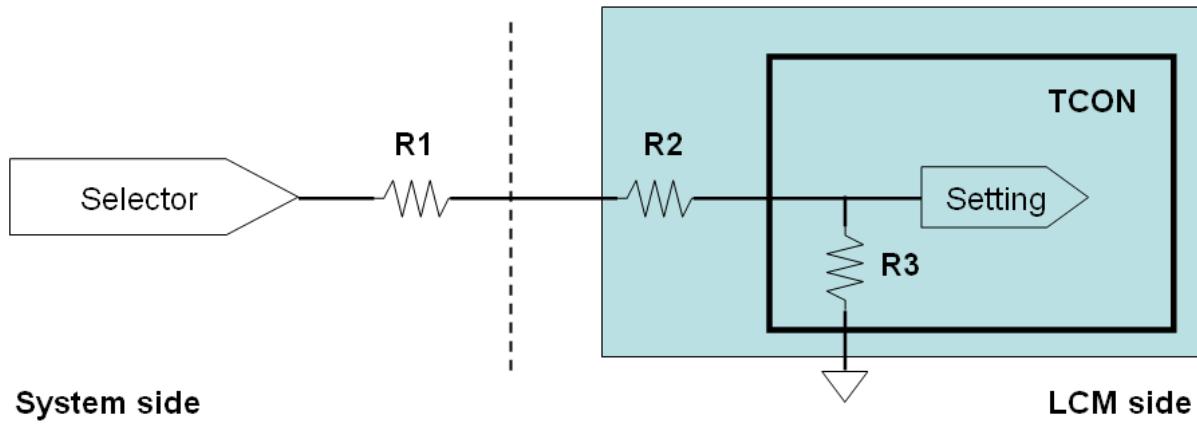
System side: R1 < 1K

Note (8) LVDS 4-port Data Mapping

Port	Channel of LVDS	Data Stream
1st Port	First Pixel	1, 5, 9, ……1913, 1917
2nd Port	Second Pixel	2, 6, 10, ….1914, 1918
3rd Port	Third Pixel	3, 7, 11, ….1915, 1919
4th Port	Fourth Pixel	4, 8, 12, ….1916, 1920

Note (9) The definition of L/R_O signal as follows

L= 0V , H= +3.3V

L/R_O	Note
L	Right glass turn on
H	Left glass turn on

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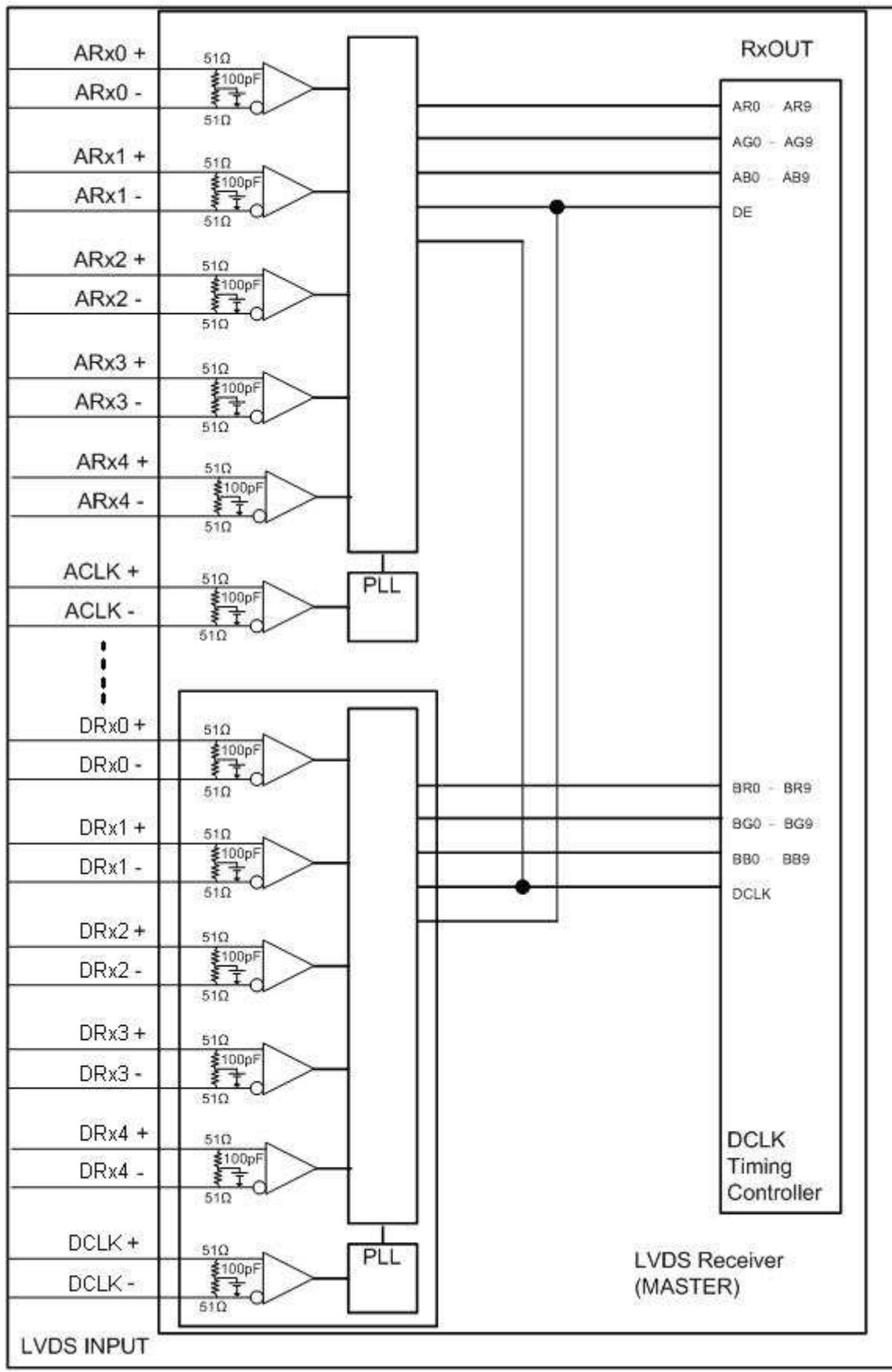
AR0~AR9: First pixel R data

AG0~AG9: First pixel G data

AB0~AB9: First pixel B data

BR0~BR9: Second pixel R data

BG0~BG9: Second pixel G data

BB0~BB9: Second pixel B data

DE: Data enable signal

DCLK: Data clock signal

The third and fourth pixel are followed the same rules.

CR0~CR9: Third pixel R data

CG0~CG9: Third pixel G data

CB0~CB9: Third pixel B data

DR0~DR9: Fourth pixel R data

DG0~DG9: Fourth pixel G data

DB0~DB9: Fourth pixel B data

Note (1) A ~ D channel are first, second, third and fourth pixel respectively.

Note (2) The system must have the transmitter to drive the module.

Note (3) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

5.2 LVDS INTERFACE

JEIDA Format : SELLVDS = L

VESA Format : SELLVDS = H or Open

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Current Cycle

VESA Format

AR 0P / AR 0N	AR0	AG0	AR5	AR4	AR3	AR2	AR1	AR0	AG0
AR 1P / AR 1N	AG1	AB1	AB0	AG5	AG4	AG3	AG2	AG1	AB1
AR 2P / AR 2N	AB2	DE	VS	HS	AB5	AB4	AB3	AB2	DE
AR 3P / AR 3N	AR6	REV	AB7	AB6	AG7	AG6	AR7	AR6	REV
AR 4P / AR 4N	AR8	REV	AB9	AB8	AG9	AG8	AR9	AR8	REV

JEIDA Format

AR 0P / AR 0N	AR4	AG4	AR9	AR8	AR7	AR6	AR5	AR4	AG4
AR 1P / AR 1N	AG5	AB5	AB4	AG9	AG8	AG7	AG6	AG5	AB5
AR 2P / AR 2N	AB6	DE	VS	HS	AB9	AB8	AB7	AB6	DE
AR 3P / AR 3N	AR2	REV	AB3	AB2	AG3	AG2	AR3	AR2	REV
AR 4P / AR 4N	AR0	REV	AB1	AB0	AG1	AG0	AR1	AR0	REV

AR0~AR9: First Pixel R Data (9; MSB, 0; LSB)

AG0~AG9: First Pixel G Data (9; MSB, 0; LSB)

AB0~AB9: First Pixel B Data (9; MSB, 0; LSB)

DE　 : Data enable signal

DCLK : Data clock signal

RSV: Reserved

5.3 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
	Data Signal — Red											**Green**										**Blue**									
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red (1021)	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (1021)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
	Green (1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	Green (1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (1021)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1
	Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

PRODUCT SPECIFICATION

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

(Ta = 25 ± 2 ºC)

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	F_{clkin} (=1/TC)	60	74.25	80	MHz	
	Input cycle to cycle jitter	T_{rcl}	-	-	200	ps	(3)
	Spread spectrum modulation range	F_{clkin_mod}	F_{clkin}-2%	-	F_{clkin}+2%	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}	-	-	200	KHz	
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	(5)
	Hold Time	Tlvhd	600	-	-	ps	

6.1.1 Timing spec for Frame Rate = 100Hz

Signal	Item		Symbol	Min.	Typ.	Max.	Unit	Note
Frame rate	2D mode		F_{r5}	94	100	106	Hz	
	3D mode		F_{r5}	100	100	100	Hz	(7)
Vertical Active Display Term	2D Mode	Total	Tv	1090	1350	1395	Th	Tv=Tvd+Tvb
		Display	Tvd	1080	1080	1080	Th	―
		Blank	Tvb	10	270	315	Th	―
	3D Mdoe	Total	Tv		1350		Th	(6),(8)
		Display	Tvd		1080		Th	
		Blank	Tvb		270		Th	
Horizontal Active Display Term	2D Mode	Total	Th	520	550	670	Tc	Th=Thd+Thb
		Display	Thd	480	480	480	Tc	―
		Blank	Thb	40	70	190	Tc	―
	3D Mdoe	Total	Th	520	550	670	Tc	Th=Thd+Thb

PRODUCT SPECIFICATION

| | | Display | Thd | 480 | 480 | 480 | Tc | — |
| | | Blank | Thb | 40 | 70 | 190 | Tc | — |

6.1.2 Timing spec for Frame Rate = 120Hz

Signal	Item		Symbol	Min.	Typ.	Max.	Unit	Note
Frame rate	2D mode		F_{r6}	114	120	126	Hz	
	3D mode		F_{r6}	120	120	120	Hz	(7)
Vertical Active Display Term	2D Mode	Total	Tv	1090	1125	1395	Th	Tv=Tvd+Tvb
		Display	Tvd	1080	1080	1080	Th	—
		Blank	Tvb	10	45	315	Th	—
	3D Mdoe	Total	Tv		1125		Th	(6), (8)
		Display	Tvd		1080		Th	
		Blank	Tvb		45		Th	
Horizontal Active Display Term	2D Mode	Total	Th	520	550	670	Tc	Th=Thd+Thb
		Display	Thd	480	480	480	Tc	—
		Blank	Thb	40	70	190	Tc	—
	3D Mdoe	Total	Th	520	550	670	Tc	Th=Thd+Thb
		Display	Thd	480	480	480	Tc	—
		Blank	Thb	40	70	190	Tc	—

Note (1)   Since the module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

Note (2)   Please make sure the range of pixel clock has follow the below equation:

$F_{clkin(max)} \geqq F_{r6} \times Tv \times Th$

$F_{r5} \times Tv \times Th \geqq F_{clkin(min)}$

PRODUCT SPECIFICATION

INPUT SIGNAL TIMING DIAGRAM
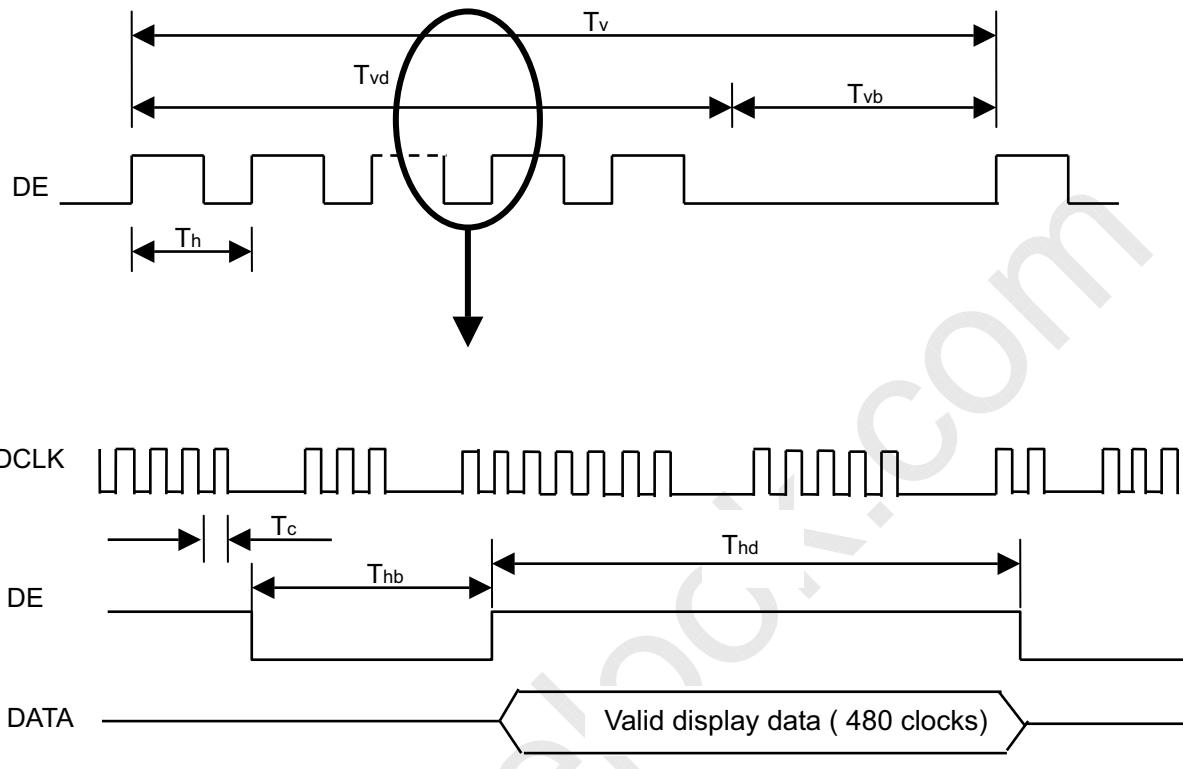
Note (3) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = I T_1 – TI
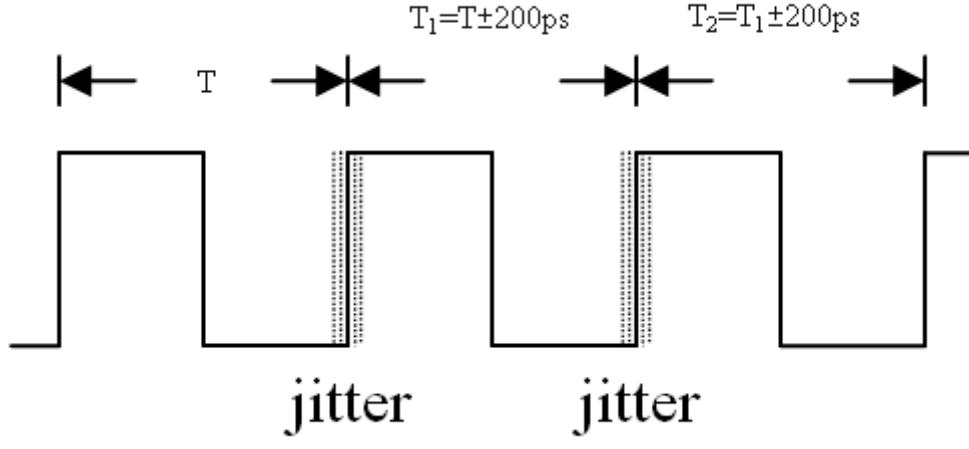
Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.
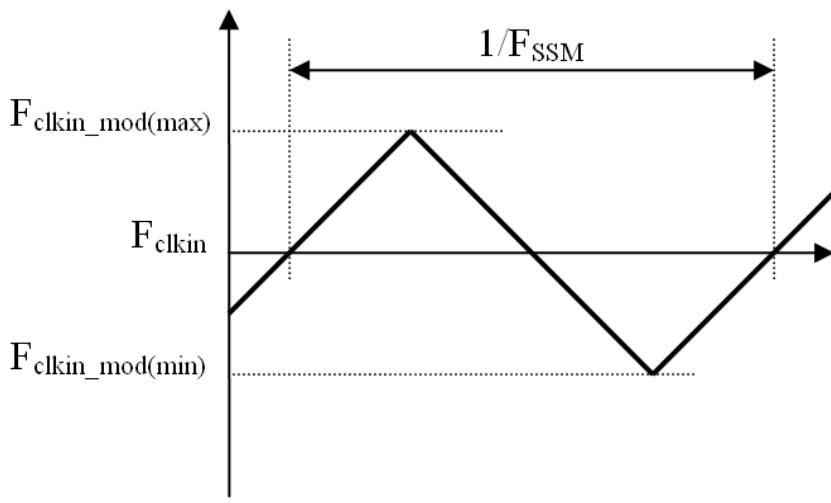
Note (5) The LVDS timing diagram and setup/hold time is defined and showing as the following figures.

LVDS RECEIVER INTERFACE TIMING DIAGRAM
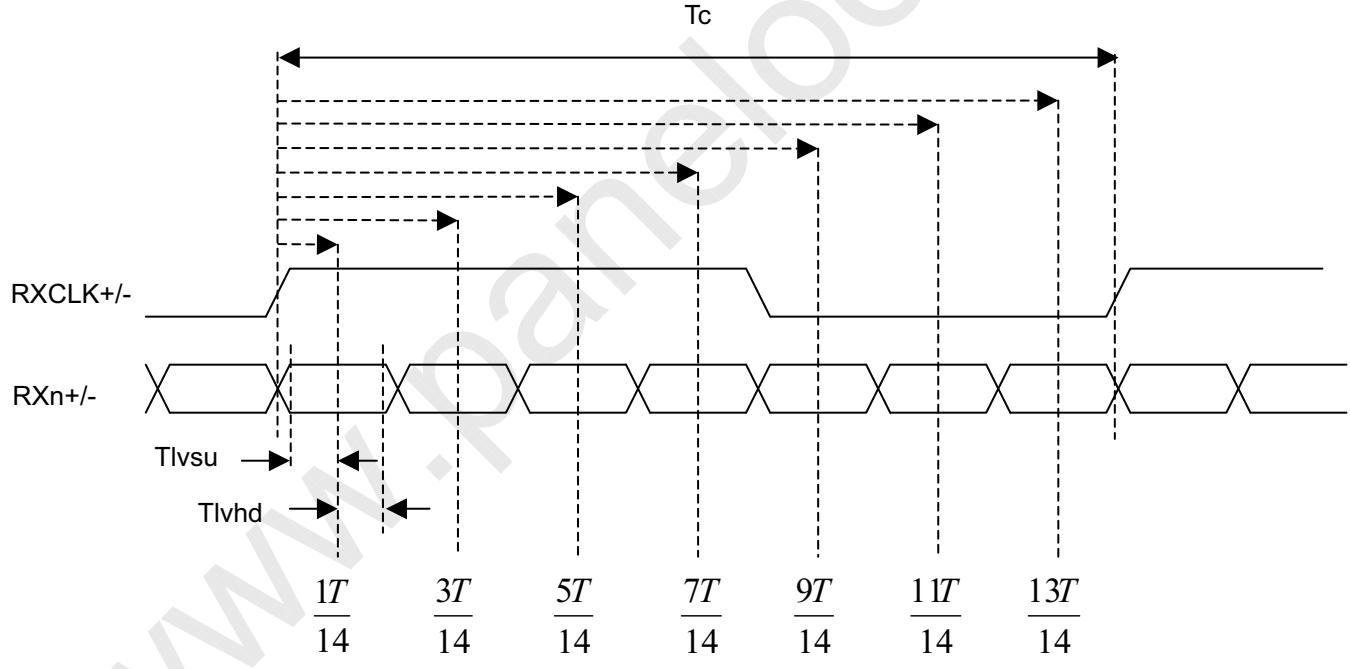
Note (6) Please fix the Vertical timing (Vertical Total =1350 / Display =1080 / Blank = 270) in 100Hz 3D mode

and Vertical timing (Vertical Total =1125 / Display =1080 / Blank = 45) in 120Hz 3D mode

Note (7) In 3D mode, the set up Fr5 and Fr6 in Typ. $\pm 3\,\mathrm{Hz}$ .In order to ensure that the electric function performance to avoid no display symptom.(Except picture quality symptom.)

Note (8) In 3D mode, the set up Tv and Tvb in Typ. ± 30.In order to ensure that the electric function performance to avoid no display symptom.(Except picture quality symptom.)

PRODUCT SPECIFICATION

6.2 POWER ON/OFF SEQUENCE (Ta = 25 ± 2 ºC)

6.2.1 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.

0V

0.1V$_{CC}$　　　　　　　　　　0.1V$_{CC}$

$0.5 \leqq T_1 \leqq 10ms$
$0 \leqq T_2 \leqq 50ms$
$0 \leqq T_3 \leqq 50ms$
$500ms \leqq T_4$

T$_1$　　　　T$_3$

T$_2$　　　　T$_4$

LVDS Signals　0V

Power On

$0 \leqq T_7 \leqq T_2$
$0 \leqq T_8 \leqq T_3$

T$_7$　　　　　　T$_8$

Option Signals
(SELLVDS,2D/3D
L/R,LD_EN)

Backlight (Recommended)
$500ms \leqq T_5$
$100ms \leqq T_6$

50%　　50%

T$_5$　　　T$_6$

Power ON/OFF Sequence

PRODUCT SPECIFICATION
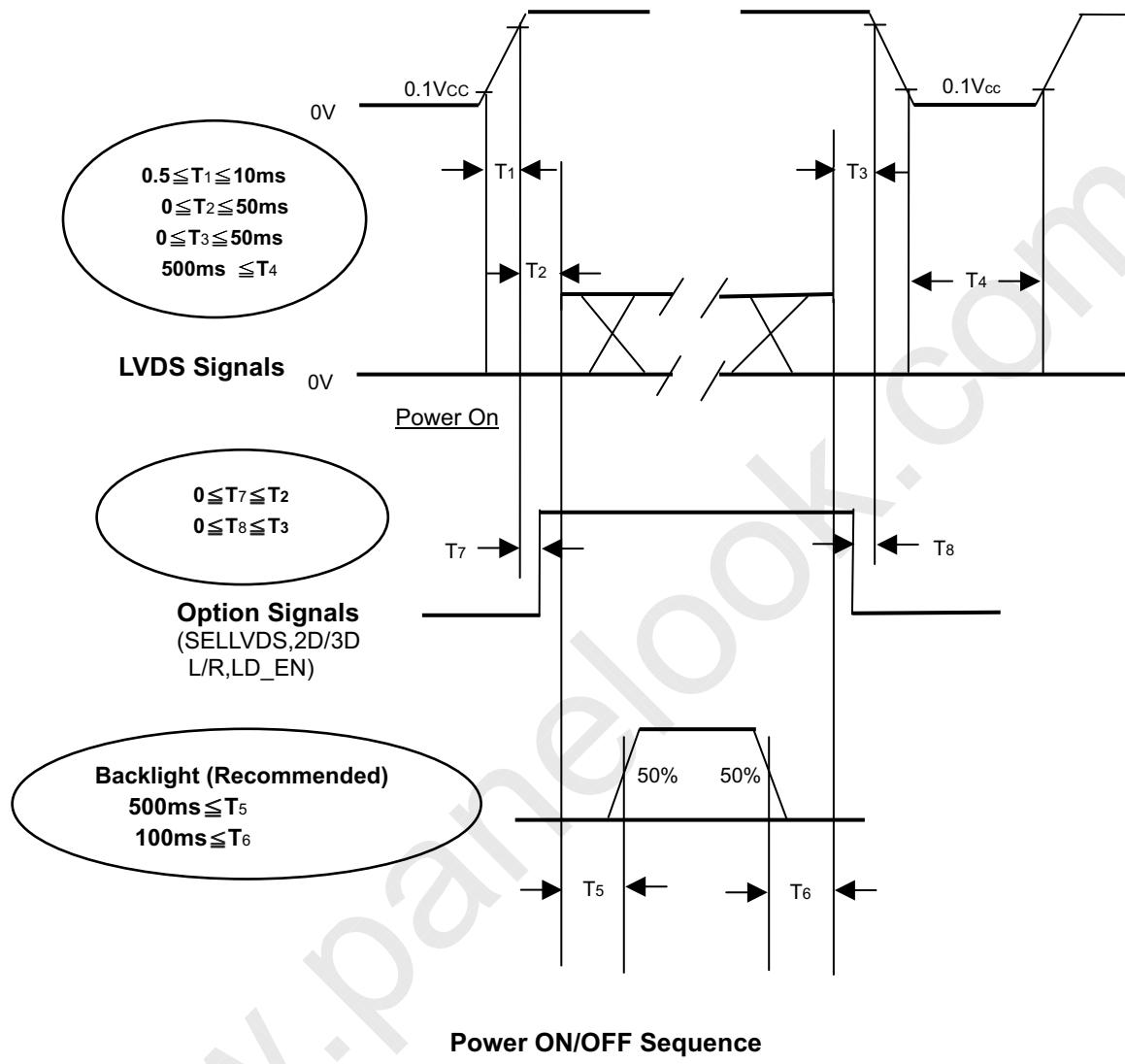
6.2.2 2D/3D MODE CHANGE2D to 3D SIGNAL SEQUENCE WITHOUT VCC TURN OFF AND TURN ON
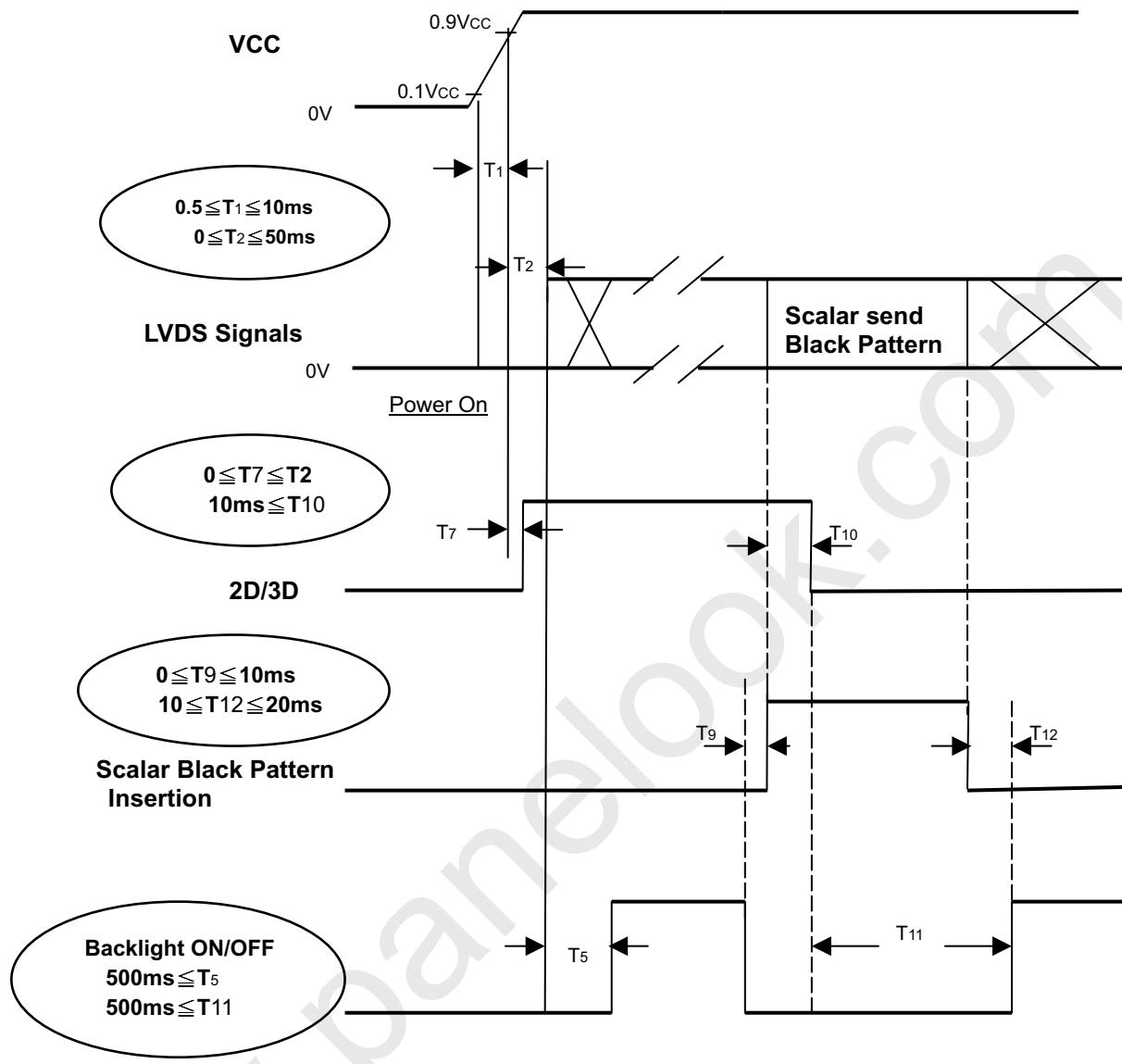
Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the LED voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance. If T2<0,that maybe cause electrical overstress failure.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

奇美電子
CHIMEI **INNOLUX**

PRODUCT SPECIFICATION

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	12V	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Current	I_L	120	mA

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring in a windless room.
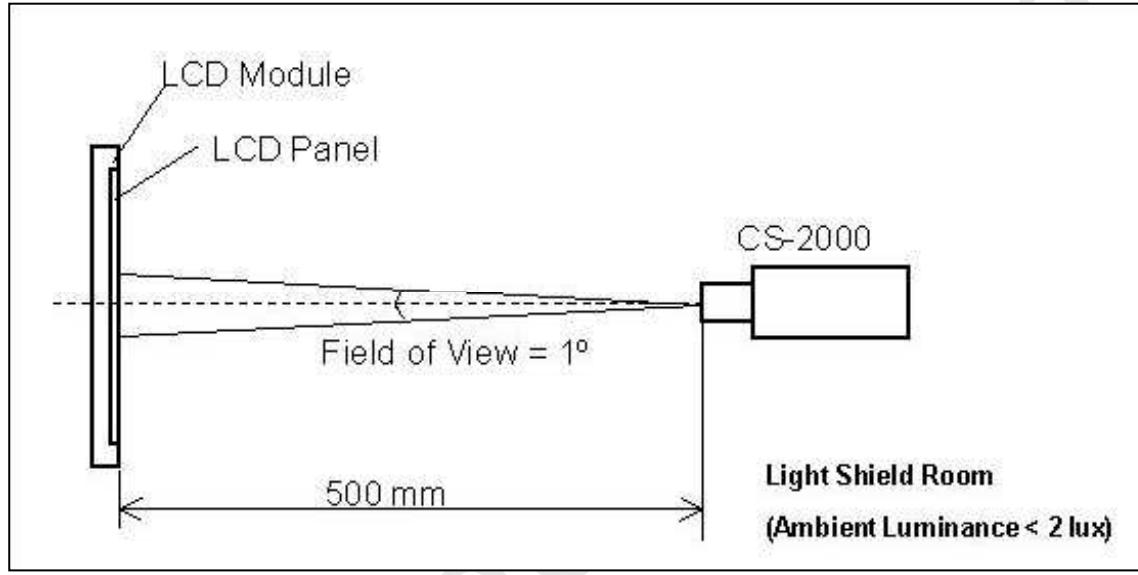
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown as below. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity	Red	Rcx	$\theta_x=0°$, $\theta_Y=0°$ Viewing Angle at Normal Direction Standard light source "C"	-	0.654	-	-	(0)
		Rcy			0.325		-	
	Green	Gcx			0.290		-	
		Gcy			0.598		-	
	Blue	Bcx			0.143		-	
		Bcy			0.089		-	
	White	Wcx			0.308		-	
		Wcy			0.359		-	
Center Transmittance		T%	$\theta_x=0°$, $\theta_Y=0°$	-	5.3	-	%	(1),(6)

PRODUCT SPECIFICATION

Contrast Ratio	CR	with CMI module		6000	-	-		(1),(3)
Response Time	Gray to gray	$\theta_x=0°$, $\theta_Y=0°$ with CMI Module		-	6	12	ms	(1),(4)
White Variation	δW	$\theta_x=0°$, $\theta_Y=0°$ with CMI module		-	-	1.3	-	(1),(5)
Viewing Angle	Horizontal	θ_x+	CR$\geq$20 With CMI module	-	88	-	Deg.	(1),(2)
		θ_x-		-	88	-		
	Vertical	θ_Y+		-	88	-		
		θ_Y-		-	88	-		

Note (0) Light source is the standard light source "C" which is defined by CIE and driving voltage are based on suitable gamma voltages. The calculating method is as following:

    1. Measure Module's and BLU's spectrum at center point. White and R,G,B are with signal input. BLU (for V546H1-LS1) is supplied by CMI.

    2. Calculate cell's spectrum.

    3. Calculate cell's chromaticity by using the spectrum of standard light source "C".

Note (1) Light source is the BLU which supplied by CMI and driving voltage are based on suitable gamma voltages.

Note (2) Definition of Viewing Angle (θx, θy):

    Viewing angles are measured by Autronic Conoscope Cono-80

Normal
$\theta x = \theta y = 0°$

$\theta y-$ $\theta y+$

$\theta x- = 90°$ x-

12 o'clock direction

$\theta y+ = 90°$

$\theta x-$ y+

$\theta x+$

6 o'clock   y-

$\theta y- = 90°$

x+ $\theta x+ = 90°$

PRODUCT SPECIFICATION
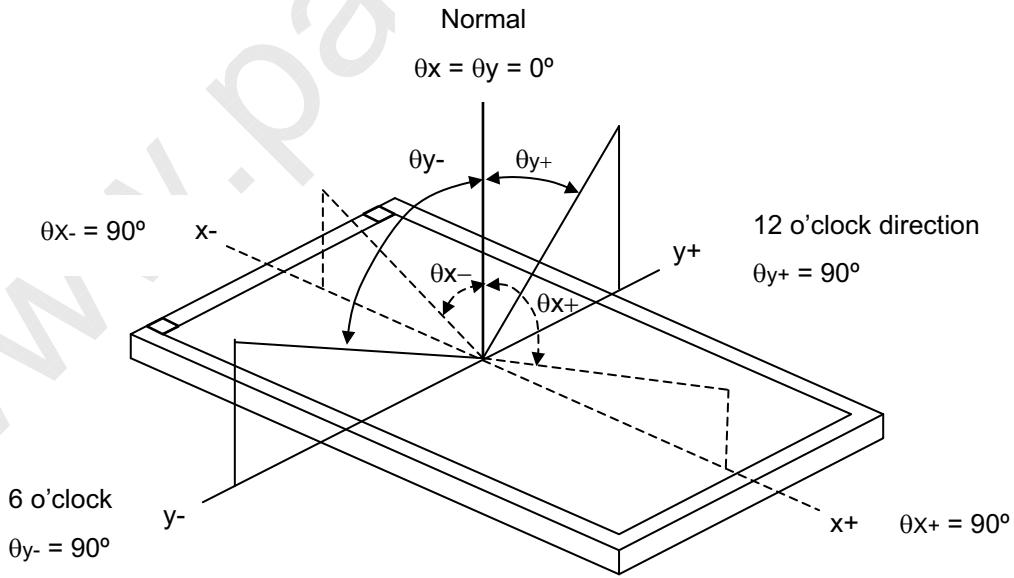
Note (3) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance of L255}}{\text{Surface Luminance of L0}}$$

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (5).

Note (4) Definition of Gray-to-Gray Switching Time:
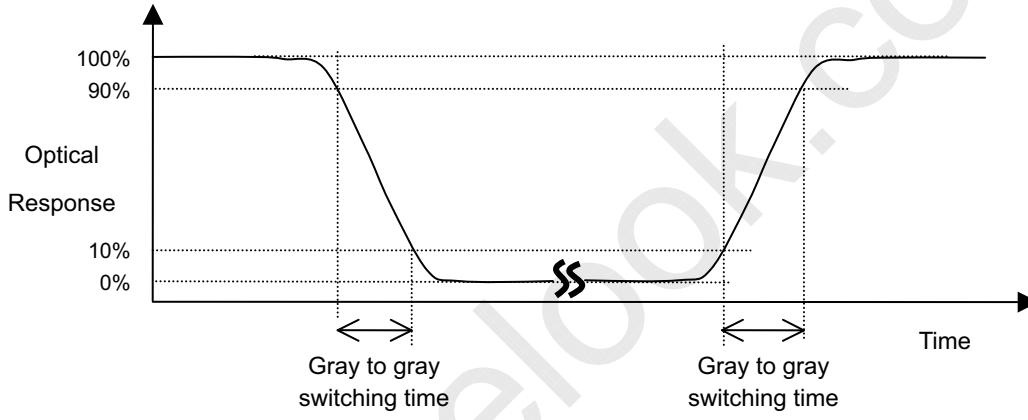
The driving signal means the signal of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023.

Gray to gray average time means the average switching time of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023 to each other.

Note (5) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]

PRODUCT SPECIFICATION

Horizontal Line

Active Area
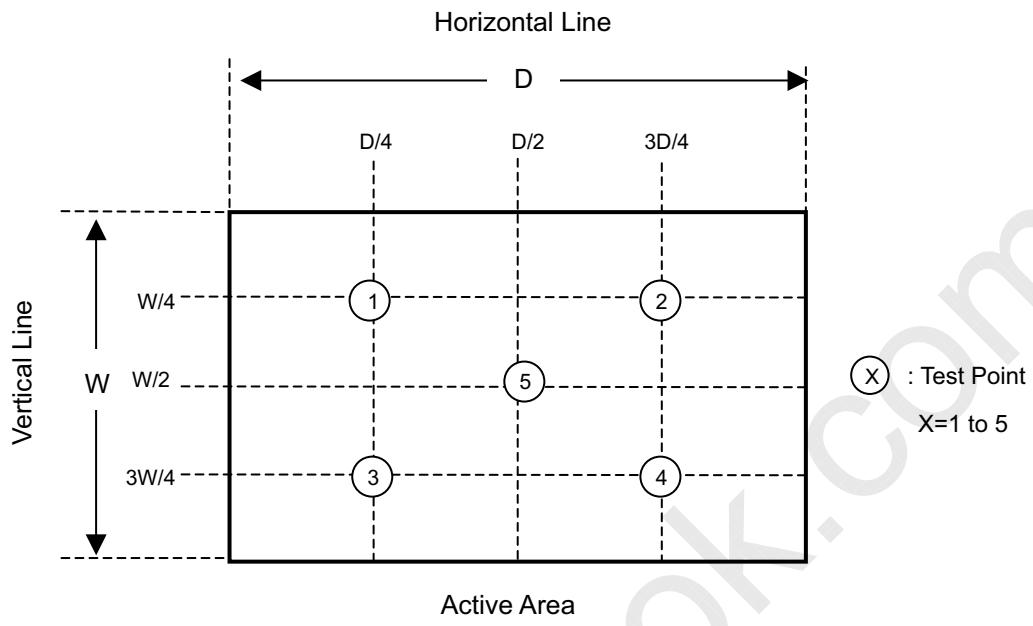
Note (6) Definition of Transmittance (T%) :

Measure the luminance of gray level 255 at center point of LCD module.

$$\text{Transmittance (T\%)} = \frac{\text{Luminance of LCD module}}{\text{Luminance of backligh unit}} \times 100\%$$

PRODUCT SPECIFICATION

8.PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

[1]   Do not apply rough force such as bending or twisting to the module during assembly.

[2]   It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

[3]   Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.

[4]   Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

[5]   Do not plug in or pull out the I/F connector while the module is in operation.

[6]   Do not disassemble the module.

[7]   Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

[8]   Moisture can easily penetrate into LCD module and may cause the damage during operation.

[9]   When storing modules as spares for a long time, the following precaution is necessary.

　　[9.1]   Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35℃ at normal humidity without condensation.

　　[9.2]   The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

[10]   When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

8.2 SAFETY PRECAUTIONS

[1]   The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.

[2]   If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

[3]   After the module's end of life, it is not harmful in case of normal operation and storage.

PRODUCT SPECIFICATION

9. DEFINITION OF LABELS

9.1 OPEN CELL LABEL

The barcode nameplate is pasted on each open cell as illustration for CMI internal contro

```
V546H1 –PS1   Rev. XX
|||||||||||||||||||||||||||||||
X X X X X X X Y M D L N N N N
```
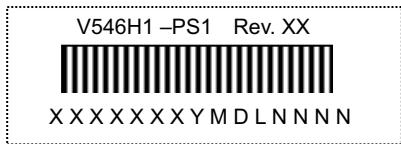
Figure.8-1 Serial No. Label on SPWB

Model Name: V546H1-PS1

Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

Serial ID: X X X X X X X Y M D L N N N N
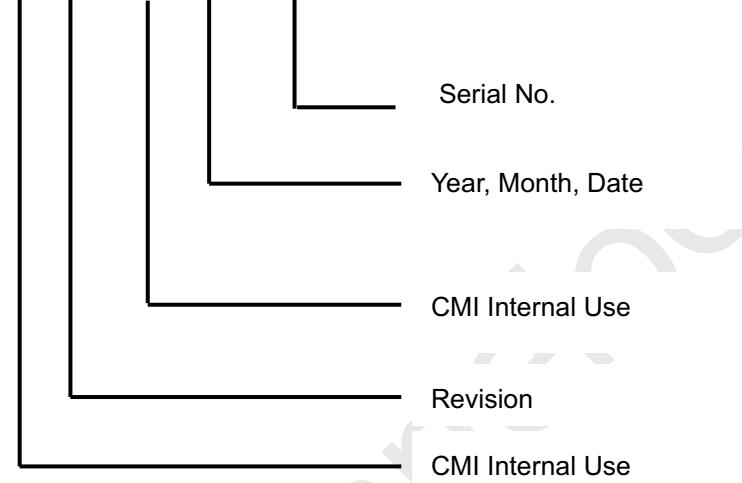
       Serial No.

       Year, Month, Date

       CMI Internal Use

       Revision

       CMI Internal Use

Serial ID includes the information as below:

Manufactured Date:

    Year: 2010=0, 2011=1,2012=2…etc.

    Month: 1~9, A~C, for Jan. ~ Dec.

    Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

Revision Code: Cover all the change

Serial No.: Manufacturing sequence of product

PRODUCT SPECIFICATION

TXXXXXXXXXXX

Figure.9-2 Panel ID Label on Cell

Panel ID Label includes the information as below:

Panel ID: T X X X X X X X X X X X X

CMI Internal Use

FAB Line: 1~8, for Fab1~Fab8

TFT

PRODUCT SPECIFICATION
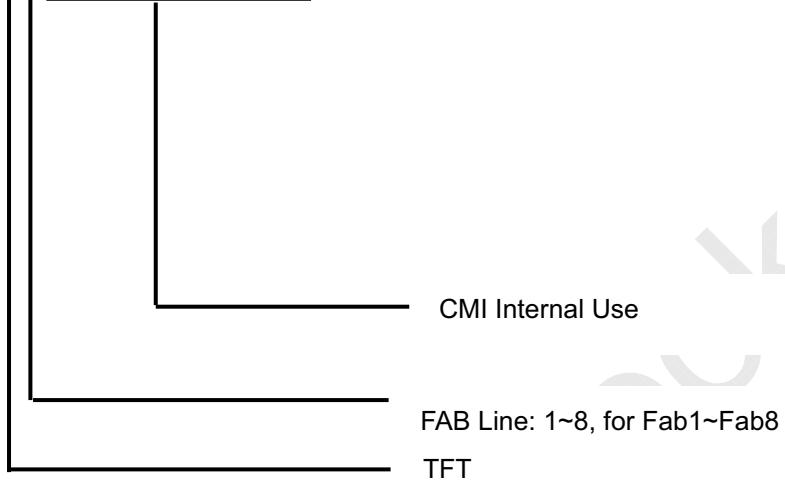
9.2 CARTON LABEL

The barcode nameplate is pasted on each box as illustration, and its definitions are as following explanation.

```
P.O. NO._____

Parts ID._____

Model Name    V546H1-PS1_____

Carton ID._____  Quantities ____
        XXXXXXXXXXXXXX

        Made In Taiwan (Made In China)
```

(a) Model Name: V546H1– PS1

(b) Carton ID: X X X X X X X Y M D X X X X
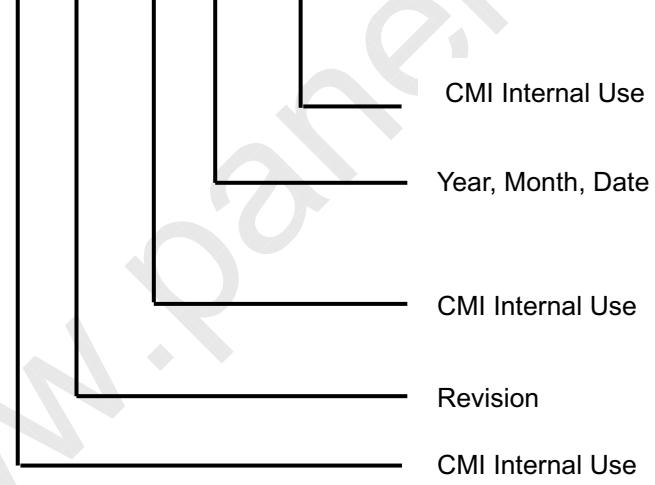
- CMI Internal Use
- Year, Month, Date
- CMI Internal Use
- Revision
- CMI Internal Use

Serial ID includes the information as below:

Manufactured Date:

Year: 2010=0, 2011=1,2012=2…etc.

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

Revision Code: Cover all the change

(c) Quantities: 8

PRODUCT SPECIFICATION

10. Packaging

10.1 PACKING SPECIFICATIONS

(1) 6 LCD TV Panels / 1 Box

(2) Box dimensions : 1454 (L) X 994 (W) X 210 (H)

(3) Weight : approximately 42Kg (6 panels per box)

10.2 PACKING METHOD

Figures 9-1 and 9-2 are the packing method
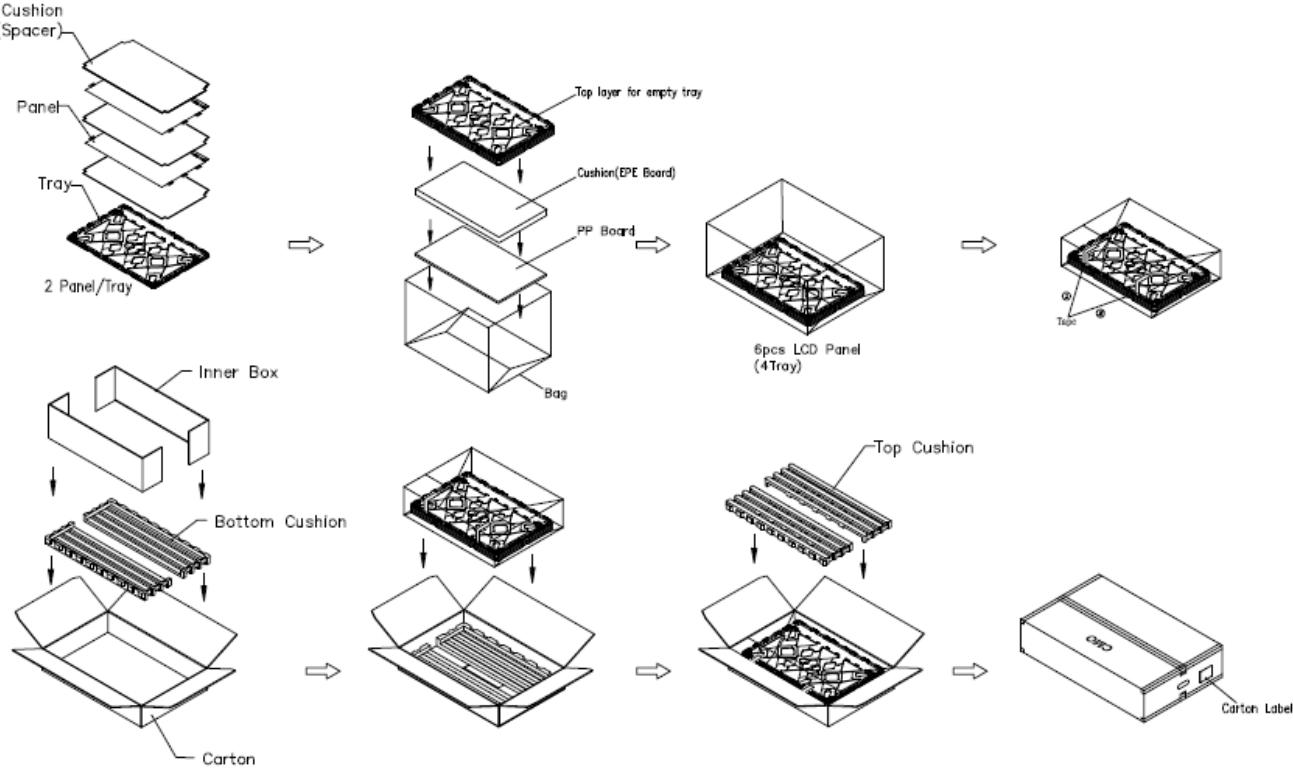
Figure.10-1 packing method

PRODUCT SPECIFICATION

Sea / Land Transportation
    (40ft HQ Container)

PE Sheet
Corner Protector
(50*50*800 mm)
Corner Protector
(50*50*800 mm)
Film
Corner Protector
(50*50*1255 mm)
t=5mm
Film
Carton Label
Pallet Label
PP Belt
Pallet
(L1490*W1150*H140mm)

Sea / Land Transportation

PE Sheet
Corner Protector
(50*50*800 mm)
Corner Protector
(50*50*550 mm)
Film
Corner Protector
(50*50*1255 mm)
t=5mm
Film
Carton Label
Pallet Label
PP Belt
Pallet
(L1490*W1150*H140mm)

Air Transportation

PE Sheet
Corner Protector
(50*50*800 mm)
Film
PP Belt
Carton Label
Pallet
(L1490*W1150*H140mm)
Pallet Label
Corner Protector
(50*50*1255 mm)
t=5mm

Version 2.0	37	Date：24 Jan 2011

PRODUCT SPECIFICATION

Uses A or the B pallet.
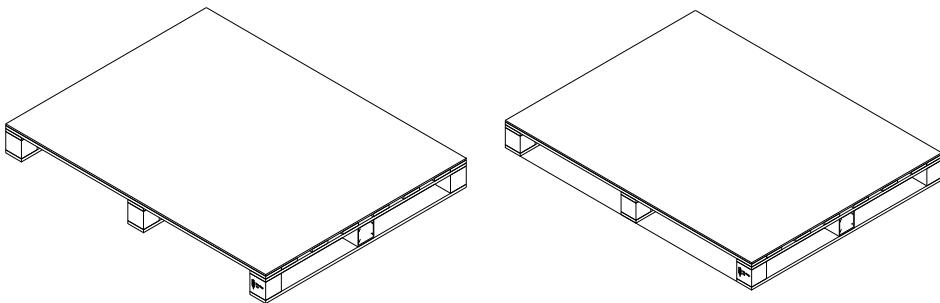
Type A   Type B

Figure. 10-2 Packing method

PRODUCT SPECIFICATION

11. MECHANICAL CHARACTERISTIC

Notes:
1.PCB_X component Height Max=10mm(Not include FFC CON, and VR)
2.Front Side Ground Need Contact with Bezel Frame
3.Back Side Ground Need Contact with Rear Frame
4.DNP:[MD]196318-60041-3
5.□ : Cu Area
6.□ : No Component Area